A Wilkinson Power Divider on a Low Resistivity Si Substrate with a Polyimide Interface Layer for Wireless Circuits

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Abstract

A 3-dB Wilkinson power divider on low resistivity silicon substrate (20 Ω-cm) with a polyimide interface layer is presented for the first time. The divider utilizes Finite Ground Coplanar (FGC) line technology, and operates at a center frequency of 15 GHz. Low insertion loss and high return loss and isolation is achieved by using a 20 μm thick polyimide interface layer on top of the silicon wafer, and a line geometry that minimizes field interaction with the lossy Si substrate. The attenuation of the FGC lines is comparable with that of thin film microstrip lines on similar substrates. Experimental and full-wave analysis results are provided.

I. Introduction

The possibility of low cost RF and microwave circuits integrated with digital and analog circuits on the same chip is creating a strong interest in silicon as a microwave substrate, especially with the development of SiGe Heterojunction Bipolar Transistors with a high frequency of oscillation [1]-[3]. The operation, however, of traditional microwave circuits, such as transmission lines, filters and antennas is problematic, due to the high loss that these circuits exhibit on low resistivity, BiCMOS and CMOS grade Si wafers.

To overcome this problem, two different approaches have been implemented. In the first approach, high resistivity Si wafers are used (ρ>2500 Ω-cm) [1]-[2], which has the advantage that traditional microwave components have a similar performance to those on insulating substrates, such as GaAs. In the second approach, dielectric layers such as polyimide are used on top of the CMOS substrate to create an interface layer that can host low loss microwave components. Both microstrip and coplanar waveguide transmission lines fabricated this way have exhibited low attenuation for an optimum polyimide thickness [4]-[5]. Recently, Finite Ground Plane (FGC) coplanar waveguide folded-slot antenna and filters have been demonstrated on such a substrate configuration with very promising results [6]-[7].

This paper presents for the first time the development of an FGC Wilkinson power divider, with a center frequency of 15 GHz on a low resistivity silicon substrate with a polyimide interface layer. Results from experimental measurements and 2.5-D Method of Moments (MoM) analysis are presented. This divider will be part of a low-cost microwave wireless communication system used to transmit data from one chip to another. This wireless interconnect scheme is proposed as an alternative to traditional conductor-based interconnects for future systems. Another application being developed is low-cost phased arrays on silicon to replace higher cost ones built on GaAs substrates.

II. Wilkinson Divider Design

a) *FGC line technology*

Finite Ground Coplanar technology was chosen for the design of the Wilkinson divider. FGC lines are similar to Coplanar Waveguide (CPW) lines, with the exception of electrically narrow ground planes. The main advantage of FGC lines is that they do not support parallel-plate modes, thus eliminating the need for via-holes between upper and lower ground planes and reducing radiation loss [8]. Experimental results have shown that a nearly TEM mode propagates over a wide frequency range (2-118 GHz), and that the total line loss depends mainly on the line geometry rather than the substrate material and thickness [8]. FGC lines are, therefore, ideal candidates for planar microwave power dividers and couplers on low resistivity Si wafers, where the conducting nature of the substrate severely limits the circuit performance.

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To design microwave power dividers on low resistivity (10-30 Ω-cm) Si wafers, the FGC electric fields must have minimum interaction with the lossy substrate. For this reason a thick layer (20 μm) of polyimide (DuPont PI 2611) is utilized on top of the silicon wafer (see Fig. 1). Previous studies have shown that it is possible to minimize the electromagnetic interaction between the FGC line and a 1 Ω-cm Si substrate if

$$(S+2W)< 3\ H_p \qquad (1)$$

where S is the center conductor width, W the slot width and H_p the polyimide thickness [9].

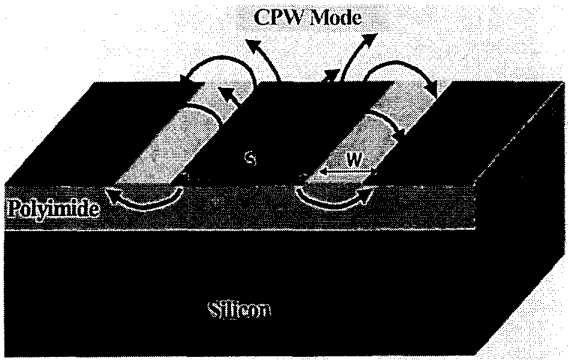

Figure 1: Schematic of FGC line on low resistivity Si wafer with a polyimide interface layer.

Two FGC line geometries for the various sections of a Wilkinson power divider are designed that yield low loss and a characteristic impedance close to either 60 Ω or 85 Ω that is required for the chosen Wilkinson divider design. Both the characteristic impedance, Zo, and effective dielectric constant, ε_{eff}, of these lines are evaluated numerically with a Method-of-Moments based software simulation tool (*Sonnet*). The substrate is low resistivity silicon (σ=5 S/m, tanδ=0.018, ε_r=11.7) with a 20 μm polyimide interface of ε_r= 3.12. Results for a frequency of 15 GHz are summarized in Table I (W_g is the ground plane width).

Dimensions (μm)	Zo (Ω)	ε_{eff}
S=75, W=23, Wg=225	62.7	2.89
S=20,W=10,Wg=200	84.3	2.26

Table 1. Simulation results for FGC lines.

As seen in Table 1, the effective dielectric constant is 2.26 for the s=20 μm, w=10 μm line indicating that the field interaction of this FGC line with the lossy Si is reduced significantly. For the first line, ε_{eff} is a bit higher indicating more interaction with the Si substrate. For minimal interaction (ideal case) an ε_{eff} of 2.06 is expected, while ε_{eff} would be 6.35 if the polyimide interface were not present.

b) Wilkinson Divider Design

A 3-dB Wilkinson power divider with a surface mount chip resistor is designed for a center frequency of 15 GHz [10]. In order to accommodate the wire bonds from the chip resistor to the center conductor of the FGC line, to minimize loss, and have an impedance value close to that of the measuring system (50 Ω), a 60 Ω FGC line with s=75 μm and w=23 μm was chosen. The two quarter-wavelength long sections of the divider have an impedance of $\sqrt{2}Z_0$=85 Ω, which yields approximately s=20 μm, w=10 μm and ε_{eff}=2.26. Based on the latter value of the effective dielectric constant, the length of the λg/4 sections is found to be 3340 μm at 15 GHz. The value of the resistor connecting these two sections is R=2Z_0=120 Ω. A schematic of the circuit can be seen in Fig. 2, while simulated results with *Sonnet* are shown in Fig. 3.

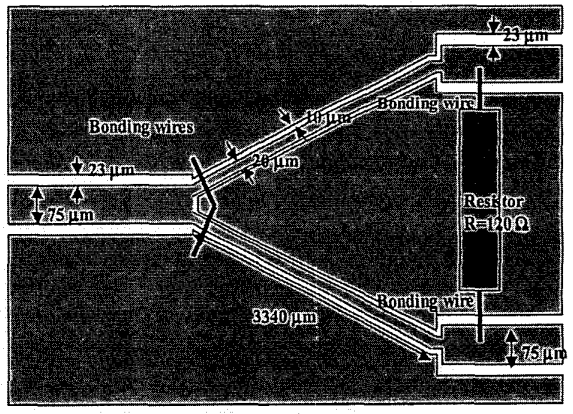

Figure 2: Schematic of the FGC Wilkinson power divider (not drawn to scale).

Simulations predict an average insertion loss of almost 5 dB, a return loss of 21 dB and an S_{23} value of -16 dB around 18 GHz. For higher frequencies the insertion loss increases, as does S_{23}. The simulations also predict an increase in the operating frequency that is due to the parasitics of

the Y-junction that are not taken into account in the original design. For the simulations the impedance of the access ports was set to 50 Ω. Figure 4 shows simulated results for the effective dielectric constant and attenuation of the s=75 μm/w=23 μm FGC line. At 18 GHz *Sonnet* predicts an attenuation of 2.50 dB/cm and an effective dielectric constant of 2.86, while at 30 GHz the values are 3.74 dB/cm and 2.83, respectively.

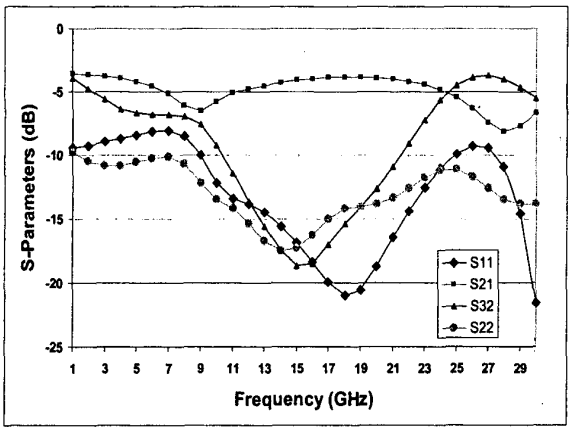

Figure 3: Simulated results for the Wilkinson divider.

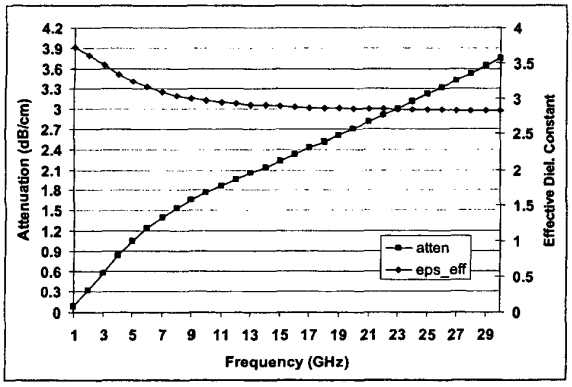

Figure 4: Simulated results of ε_{eff} and Zo for the FGC line with s=75 μm, w=23 μm.

III. Fabrication

On 20 Ω-cm silicon wafers, four layers of DuPont PI 2611 polyimide are deposited and cured to a thickness, Hp, of 20 μm. FGC circuits are fabricated on top the polyimide using standard liftoff processing with the FGC made of 0.02 μm of Ti and 1.5 μm of evaporated gold. No backside ground plane or Si passivation layers are grown. The surface mount resistor is bonded to the ground plane between the two output ports with silver epoxy glue. Two 0.007-inch Au bond wires are used at each terminal of the resistor to make the connections to the center conductor of the FGC line. Bond wires are also used to connect the ground planes at each right angle bend and the Y-junction to equalize the ground plane potentials and eliminate the slotline mode.

The FGC propagation characteristics are measured with a vector network analyzer and probe station. A quartz spacer between the Si substrate and the probe station wafer chuck is used to eliminate parasitic microstrip and parallel plate waveguide modes during testing. The propagation constant, $\gamma=\alpha+j\omega\sqrt{\varepsilon_{eff}}/c$ where α is the attenuation constant, ω is the angular frequency, and c is the velocity of light in vacuum, is deembedded through the Thru-Reflect-Line (TRL) calibration routine implemented in the software program MULTICAL [11]. For each FGC line characterized, four delay lines with the longest line being 1 cm are used in addition to the thru line to enhance accuracy from 1 to 30 GHz. The reference planes are set by the calibration to the Y-junction at port 1 and at a point 2500 μm from the output ports of the Wilkinson divider.

IV. Results

Figure 5 shows the measured effective dielectric constant and attenuation for the FGC lines with s=75 μm, w=23 μm. The constant behavior of ε_{eff} in Fig. 5, indicates the propagation of a nearly pure TEM mode for both FGC line geometries. ε_{eff} is approximately 2.9 for the s=75/w=23 μm line indicating that it has a small interaction with the Si substrate and is in excellent agreement with the simulated value of 2.89. Regarding attenuation, the s=75/w=23 μm line has a very good behavior with an attenuation of 3.37 dB/cm at 20 GHz, which is a bit higher than the predicted value but within the expected error considering the difficulty in simulating attenuation.

Measured results for the Wilkinson divider are shown in Fig. 6, and agree well with the simulated ones shown in Fig. 3. The measured insertion loss is higher than the simulated loss for frequencies above 24 GHz, due to the non-efficient modeling of the frequency-dependent variation of the conductivity (quasi-static loss approach)

implemented by *Sonnet*. At 18 GHz the divider exhibits a loss of approximately 8 dB, while at 20 GHz the loss is only 6.8 dB, which includes 0.83 dB of insertion loss due to the 2500 μm of extra line length at the two output ports. Thus, the divider circuit has an insertion loss of 6 dB (6.83-0.83 dB), which agrees well with the predicted value of 5 dB. The return loss both for ports 1 and 2 is around 14 dB at 20 GHz while the isolation between the two output ports is higher than 10 dB for the entire measured band. At 20 GHz the measured isolation is 16 dB.

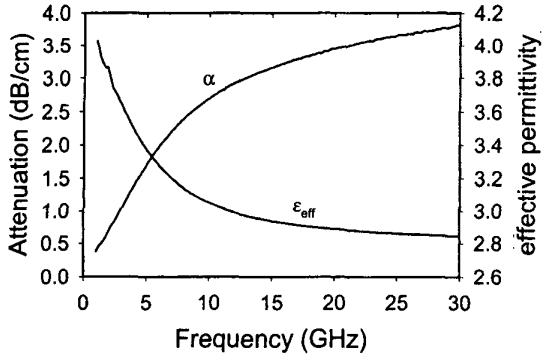

Figure 5: Measured attenuation and effective dielectric constant for FGC lines with s=75 μm, w=23 μm and w_g=225 μm.

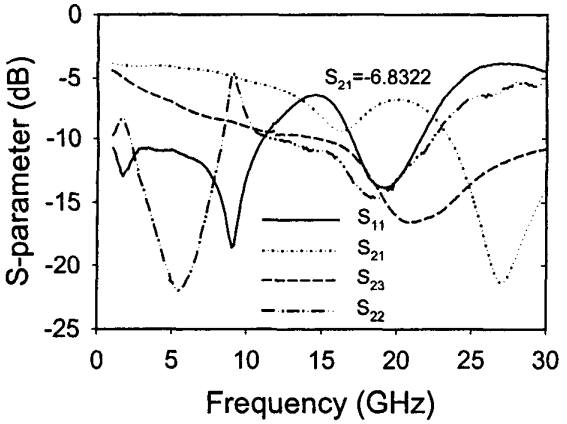

Figure 6: Measured results for the Wilkinson power divider from 10 to 30 GHz.

V. Conclusions

A Wilkinson power divider, on a low resistivity silicon substrate with a polyimide interface layer has been designed, fabricated and tested. To the author's knowledge this is the first demonstration of such a microwave circuit. The divider response agrees well with simulated results and exhibits a 6 dB insertion loss and 14 dB return loss at 20 GHz. Isolation between the output ports is 16 dB at 20 GHz. The Wilkinson power divider will be part of a wireless chip-to-chip interconnect system, as well as other wireless microwave systems built on low cost CMOS grade wafers.

Acknowledgements

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